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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/068,628 | 02/06/2002 | Shin Kim | 9898-206 | 6784 |

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| EXAMINER |
|---|
| DINH, TUAN T |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/068,628 | KIM ET AL. | |
| | Examiner | Art Unit | |
| | Tuan T Dinh | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-14,20 and 21* is/are pending in the application.

4a) Of the above claim(s) *15-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "**gate dielectric layer and a gate electrode**, claim 21, line 2" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Applicant should provide **a cross-hatching** of materials in figures 1-3, for example: first, second, or an inner dielectric layers.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 21 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification is silent regarding "the substructure comprises a gate dielectric layer and a gate electrode, claim 21, lines 1-2".

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 9, 12-14, and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien (U. S. Patent 5,723,822) in view of Zambrano (U. S. Patent 5,773,899).

As best understood to claims 20-21, Lien discloses a bonding pad of a semiconductor device (chip), column 1, lines 10-11, as shown in figure 1 comprising:

a semiconductor substrate (101, column 1, line 15) capable of being a substructure;

a first dielectric layer (104, column 1, lines 16-17) formed on the substructure (101);

a polysilicon film plate (105, column 1, line 17) formed on the first dielectric layer (104) and configured to improve the resistance of the bonding pad to stress created during wire bonding (114, column 1, lines 18-19);

a first metal layer (110, column 1, line 30) formed on the polysilicon film plate (105), wherein the first metal layer is formed having a recessed area;

a second metal layer (111; 112, column 1, line 30) formed on the first metal layer (110) wherein a portion of the second metal layer is arranged within the recessed area

of the first metal layer to improve the resistance of the bonding pad to stress (see figure 1); and

a activation layer (109, column 1, line 48) formed overlying the second metal layer (111; 112) having an opening (115, column 1, line 49) that exposes the second metal layer as a bonding pad (see figure 1).

Lien does not disclose a substructure formed on a semiconductor substrate. Zambrano shows a bonding pad for a semiconductor ship as shown in figure 1 comprising a substructure (2) formed on a semiconductor substrate (3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a substructure formed on a substrate as taught by Zambrano to employ the bonding pad of the semiconductor device of Lien in order to improve mechanical strengths laminated of layer for a semiconductor device.

As to claims 1, and 13-14, Lien discloses a bonding pad of a semiconductor device or chip as shown in figure 1 comprising:

a semiconductor substrate (101) capable of being a substructure;

a first dielectric (104) layer formed on the substructure;

a polysilicon film plate (105) formed on the first dielectric layer (104) and configured to improve the resistance of the bonding pad to stress induced during wire bonding (114);

a second dielectric layer (106) formed overlying the polysilicon film plate, the second dielectric layer (106) having a first opening that exposes a region of the polysilicon film plate;

a first metal layer (110) formed on the polysilicon film plate (105) through the first opening;

an inner metal dielectric layer (107-108) formed overlying the first metal layer (110), the inner metal dielectric layer (107-108) having a second opening

a second metal layer (112) formed on the first metal layer (110); and

a passivation layer (109, column 1, line 48) formed overlying the second metal layer (111; 112) having an opening (115, column 1, line 49) that exposes the second metal layer as a bonding pad (see figure 1).

Lien does not disclose a substructure formed on a semiconductor substrate. Zambrano shows a bonding pad for a semiconductor ship as shown in figure 1 comprising a substructure (2) formed on a semiconductor substrate (3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a substructure formed on a substrate as taught by Zambrano to employ the bonding pad of the semiconductor device of Lien in order to improve mechanical strengths laminated of layer for a semiconductor device.

As to claims 2 and 4, Lien discloses a bonding pad of a semiconductor device as shown in figure 1 wherein the first and second metal layers are formed having a somewhat horseshoe-shaped cross-section.

As to claim 3, Lien discloses a bonding pad of a semiconductor device as shown in figure 1 wherein a region of the second metal layer (112) is disposed within a recessed area of the first metal layer (110).

As to claim 5, Lien discloses a bonding pad of a semiconductor device as shown in figure 1 wherein the substructure comprises circuitry configured to provide a dynamic random access memory (column 1, line 25).

As to claim 9, Zambrano discloses a bonding pad of a semiconductor device as shown in figures 1-7 wherein the first and second metal layers (12, 16) are formed of aluminum (column 3, lines 21, and 31-32).

It would have been obvious to have aluminum layers as taught by Zambrano to employ the semiconductor package of Lien in order to improve an insulation of the package.

As to claim 12, Lien discloses a bonding pad of a semiconductor device as shown in figure 1 wherein the wire bonding (114) is beam lead bonding.

6. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien ('822) in view of Zambrano ('889) and further in view of Fukumoto (U. S. Patent 6,307,264).

As to claim 6, Lien and Zambrano disclose all of the limitations of the claimed invention, except for the first dielectric layer being a boron phosphor silicate glass (BPSG) layer.

Fukumoto teaches a dielectric layer (4) made of boron phosphor silicate glass disclosed in figures 1-3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use BPSG layer as taught by Fukumoto to employ the bonding

pad structure of Lien and Zambrano in order to provide a thermal insulation and an electrical conductivity.

As to claims 7, Lien and Zambrano disclose all of the limitations of the claimed invention, except for the first dielectric layer having a thickness of about 0.3-0.4 micrometers (10,000 angstroms = 1 micrometer).

Fukumoto shows a semiconductor device comprising a dielectric layer (47) having a thickness about 0.3-0.4 micrometers (column 6, lines 28-35).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have Tawas's teaching to employ the package of Lien and Zambrano in order to improve a profile and an insulation of the semiconductor package.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lien ('822) in view of Zambrano ('889) and further in view of Takes et al. (U. S. Patent 6,369,409).

As to claim 8, Lien and Zambrano disclose all of the limitations of the claimed invention, except for the polysilicon film plate having a thickness of about 0.1-0.2 micrometers (10,000 angstrons = 1 micrometer).

Takasu shows a semiconductor device comprising a polysilicon film plate (105-107) having a thickness about 0.1-0.2 micrometers (column 4, lines 61-62).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have Takasu's teaching to employ the package of Lien and Zambrano for purpose of improve a high resistance value for semiconductor package.

8. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lien ('822) in view of Zambrano ('889) and further in view of Gotoh et al. (U. S. Patent 6,204,454).

As to claims 10-11, Lien and Zambrano disclose all of the limitations of the claimed invention, except for the metal layer having a thickness of about 0.7-0.9 micrometers (10,000 angstrons = 1 micrometer).

Gotoh shows a semiconductor device comprising a metal layer (102) having a thickness about 0.7-0.9 micrometers (column 1, lines 51-52).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have Gotoh's teaching to employ the package of Lien and Zambrano in order to reduce a size of semiconductor package.

### *Response to Arguments*

9. Applicant's arguments with respect to claims 1-14, and 20-21 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

**TD**
February 12, 2003

DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
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